[redacted]

This course covers NXP G4+ Power CPU, including MPC7448

Objectives

- The course provides coding guidelines based on the knowledge of the instruction pipeline.
- Alignment rules are to be determined to avoid cache replacement of data being processed.
- Data flows between SDRAM, L1 caches , L2 and possibly L3 cache are highlighted.
- MESI cache coherency protocol is introduced in increasing depth.
- Vector instructions and new C operators are viewed in detail.
- Data streams parameterizing is emphasized through an example.
- This course covers bus operation in either 60X or MPX mode.
- Through a FIR algorithm, the instructor shows how to vectorize processing and reduce execution time using data streaming.
- The internal performance monitor has been programmed so that different versions of the FIR algorithm implementation can be compared.
- This course has been delivered several times to companies involved in the design of avionics equipments, such as flight controller.

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

PIPELINE

- Pipeline basics
- 744X/5X pipeline implementation
- Issue queue resource requirements
- Execution model
- Dispatch conditions, completion conditions
- Execution serialization
- Branch management
- Guarded memory

L1, L2 and L3 CACHES

- Cache basics
- 744X/5X L1 cache
- Transient load instructions benefits
- L2 cache organization
- L2 replacement algorithm selection, L2 locking
- L3 Cache organization according to L3 size
- L3 replacement algorithm selection, L3 locking
- L3 SSRAM used as private memory
- Cache coherency basics
- The MESI L1 data line states
- MESI snooping sequences involving 2 G4 and a PCI master

INTERNAL DATA FLOWS

- L1 and L2 cache loading, hit under miss
- The MSS [Memory Sub System]
- The load fold queue
- The store miss merging advantage
- Purpose of sync and eieio instructions

MPC744X/5X SPECIFIC UNITS

- The 3 architecture layers introduction : UISA, VEA and OEA
- Low power modes
- Performance monitor
- JTAG debugger
- Real time trace
- Differences between 7441, 7445, 7450, 7451, 7455, 7447, 7457 and 7448

THE UISA LAYER

- Branch instructions
- Integer load / store instructions
- Integer arithmetic and logic instructions
- IEEE754 basics
- Float load / store instructions
- Float arithmetic instructions
- The EABI

THE VEA LAYER

- Cache related instructions
- Little-endian emulation

- PowerPC timers : TB and DEC

ALTIVEC IMPLEMENTATION

- Altivec introduction, SIMD processing
- Intra vs inter element instructions
- Altivec registers
- ANSI C extension to support vector operators
- Vector load / store instructions
- Vector integer instructions
- Vector float instructions
- Vector permut instructions
- Altivec implementation on the 744X/5X
- Data streams management
- EABI extension to support Altivec

THE OEA LAYER - MMU

- MMU goals
- The PowerPC address processing
- Enabling of 4 additional BAT on 7445/55
- 32-bit or 36-bit real address size selection
- WIMG attributes definition, page and block access rights definition
- Process protection through VSID selection
- TLB organization
- Page translation
- Software vs hardware TLB reload
- MMU implementation in real-time sensitive applications

THE OEA LAYER EXCEPTION MECHANISM

- Exception management
- Registers updating related to the exception cause
- Requirements to support exception nesting

MPC744X/5X HARDWARE IMPLEMENTATION

- Bus interface configuration
- Auto-check on power up
- Pinout
- Bus features : address pipelining, split transactions
- 60X bus mode : address phase and data phase
- MPX bus mode : *HIT and *DRDY pins use
- Data only transactions
- MPX bus cycles overview
- Other signals : interrupts, machine check
- Synchronous SRAMs technologies
- L3 bus pinout, L3 clock synchronization
- SSRAM related parameters initialization in L3CR register

Renseignements pratiques

Inquiry : 5 days