This course covers NXP G4 Power CPUs

Objectives

- The course provides coding guidelines based on the knowledge of the instruction pipeline.
- Data flows between SDRAM, L1 caches and L2 cache are highlighted.
- Cache coherency protocol is introduced in increasing depth.
- Vector instructions and new C operators are viewed in detail.
- Data streams parameterizing is emphasized through an example.
- This course covers bus operation, either 60X or MPX mode.
- Through a FFT algorithm, the instructor shows how to vectorize processing and reduce execution time using data streaming.
- The internal performance monitor has been programmed so that different versions of the FFT algorithm implementation can be compared.

A more detailed course description is available on request at formation@ac6-formation.com

Prerequisites

- Experience of a 32 bit processor or DSP is mandatory.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

MPC7400/10 PIPELINE

- Superscalar out-of-order execution
- Branch Target Instruction Cache
- Static vs dynamic branch prediction
- Coding guidelines

L1 AND L2 CACHES

- Cache basics
- PLRU L1 replacement algorithm, FIFO L2 replacement algorithm
- Hardware data cache flush
- Cache coherency based on snooping, the MEI, MESI and MERSI state machines

INTERNAL DATA FLOWS

- Data and instructions queuing mechanism to decouple bus operation and internal activity
- The Memory Sub System
- The load fold queue and the store miss merging

MPC7400/10 SPECIFIC UNITS

- Power management
- Performance monitor
- JTAG debugger
- Differences between 7400 and 7410

THE UISA LAYER

- User registers
- Branch instructions
- Integer instructions
- IEEE754 floating point standard
- Float instructions
- EABI introduction

THE VEA LAYER

- Cache related instructions
- Little-endian emulation
- PowerPC timers

ALTIVEC IMPLEMENTATION

- Altivec registers
- Vector load / store instructions
- Vector integer instructions
- Vector float instructions
- Vector permut instructions
- ANSI C extensions to support vectors
- Altivec implementation on 7400/10
- Data streams

THE OEA LAYER - MMU

- MMU goals

- Process protection
- Tablesearch, hash value
- MMU implementation in real-time sensitive applications

THE OEA LAYER EXCEPTION MECHANISM

- Supervisor registers
- Context saving through SRR0/SRR1 registers
- Handler table
- Exception nesting

MPC7400 HARDWARE IMPLEMENTATION

- Auto-check on power up
- Bus features : address pipelining, split transactions
- 60X bus cycles
- MPX data only transactions
- Synchronous SRAM technologies
- L2 bus interface

Renseignements pratiques

Inquiry : 5 days