This course covers the Display Serial Interface V1.1 (DSI 1.1)

Objectives

- The course starts with an overview of MIPI specification.
- The layers are described using a bottom-top approach, starting with D-PHY and ending with DSI.
- Forward and Reverse capabilities of a D-PHY are studied.
- The course details the electrical characteristics of D-PHY.
- Access to configuration and status registers through Reverse direction is covered.
- Multi-lane distribution and merging of packets is explained.
- The course focuses on the low level protocol, based on short and long packets used to transport images, embedded data and framing informations.
- Data formats and possible compression of raw data is detailed to understand how the long packet payload is organized.
- Companies interested in attending this course must adhere to MIPI organization.
- This course has been designed for engineers in charge of SoC architecture, functional verification or silicon validation.

A more detailed course description is available on request at training@ac6-training.com

Prerequisites

- Basic knowledge on video transport.

Course Environment

- Theoretical course
  - PDF course material (in English) supplemented by a printed version for face-to-face courses.
  - Online courses are dispensed using the Teams video-conferencing system.
  - The trainer answers trainees' questions during the training and provide technical and pedagogical assistance.
- At the start of each session the trainer will interact with the trainees to ensure the course fits their expectations and correct if needed

Target Audience

- Any embedded systems engineer or technician with the above prerequisites.

Evaluation modalities

- The prerequisites indicated above are assessed before the training by the technical supervision of the traineein his company, or by the trainee himself in the exceptional case of an individual trainee.
- Trainee progress is assessed by quizzes offered at the end of various sections to verify that the trainees have assimilated the points presented
- At the end of the training, each trainee receives a certificate attesting that they have successfully completed the course.
  - In the event of a problem, discovered during the course, due to a lack of prerequisites by the trainee a different or additional training is offered to them, generally to reinforce their prerequisites,in agreement with their company manager if applicable.

Plan

INTRODUCTION TO MIPI SPECIFICATIONS

D-PHY

- Universal lane module architecture
- Control character usage
- Uni-directional data lanes
- Bi-directional data lanes, turnaround procedure
- Clock lane
- High-Speed data transmission in bursts
- System power states
- Low power states, escape mode
- Low power data transmission
- High-Speed clock transmission
- Fault detection

DISPLAY COMMAND SET (DCS)

- Display architecture
- Power level definition
- Self-diagnostic functions
- Command description
- Pixel-to-byte mapping

DISPLAY SERIAL INTERFACE (DSI)

- Overview
- Physical layer, flow control
- Multi-Lane Distribution and Merging
- Low-Level Protocol Errors and Contention
- DSI protocol
- DSI conformance test suite
- DSI interoperability test suite

Renseignements pratiques

Inquiry : 1 day